C3NiT - Janzén

Kompetenscentrum

Centre for III-nitride technology

C3NiT Day 11 Nov 2020

Improve Passivation, Ohmic Contacts, and QuanFINE for High-Frequency Applications

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VINNOVA

SiN Passivation by MOCVD and LPCVD (VINNOVA SME Project)

Motivation

Understanding the relationship of device performance to the following parameters:

- SiN/epi interface properties (HR-STEM and XPS)
- Refractive index (Ellipsometry)
- Strain of SiN and epi (XRD and Surface Profiler) => Impact 2DEG
- Binding energy for different atoms (XPS) => Impact trap states

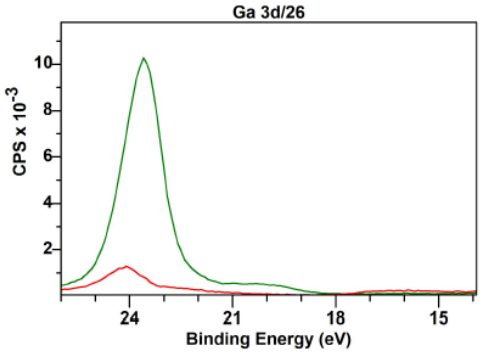
Summary

- Larger shifting of Ga-binding energy is revealed on LPCVD SiN

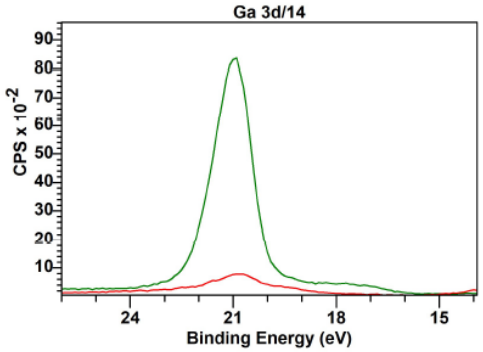
Future Work

- A low trapping in-situ MOCVD SiN
- The correlation between device performance and parameters stated above

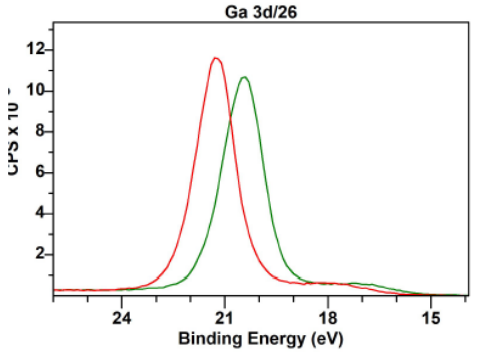
LPCVD SiN n=2.0



MOCVD SiN n=2.0



Epi Without SiN



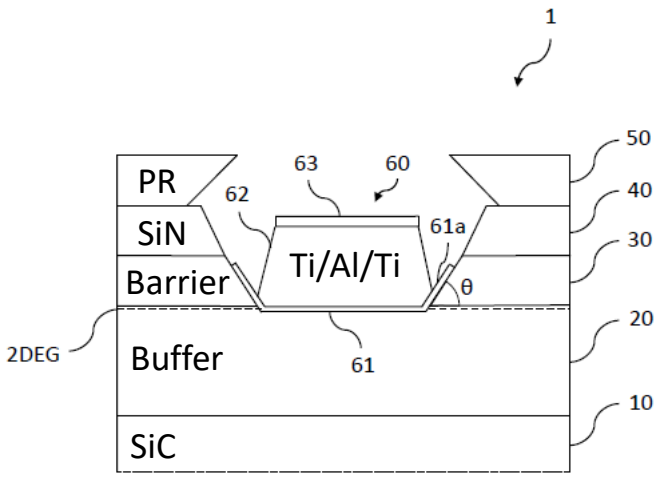
Low Temperature Ti-based Deeply Recessed Sidewall Ohmic Contacts (Patent Submitted)

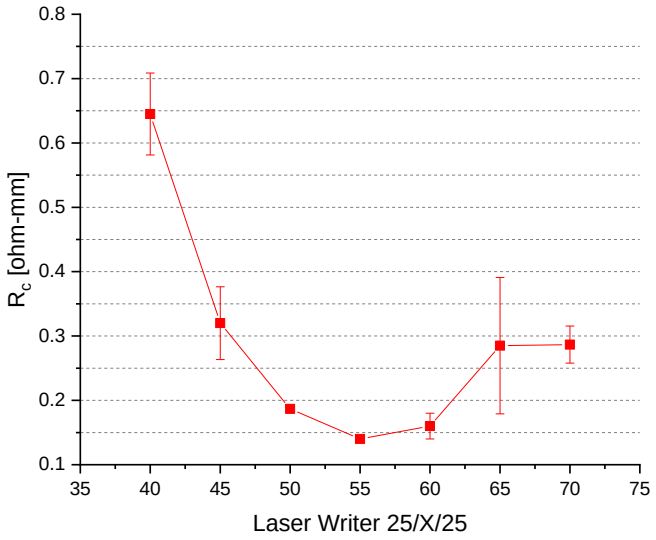
Achievement

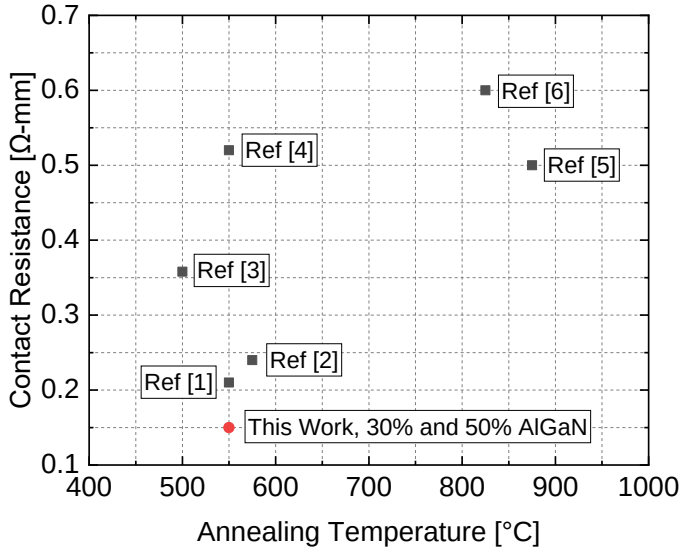
- Low annealing temperature: 550-600 C
- Ti/Al/Ti metal stacks is similar to conventional Ti/Al/Ni/Au
- High Al content barrier (30% and 50%) with record low contact resistance: < 0.2 ohm-mm
- Shorter annealing time (550 C, <8 mins) than low temperature Ta ohmic contacts (550C, 40-56 mins)

Future Plan

- High uniformity contact resistance on 4” wafer
- On pure AlN barrier







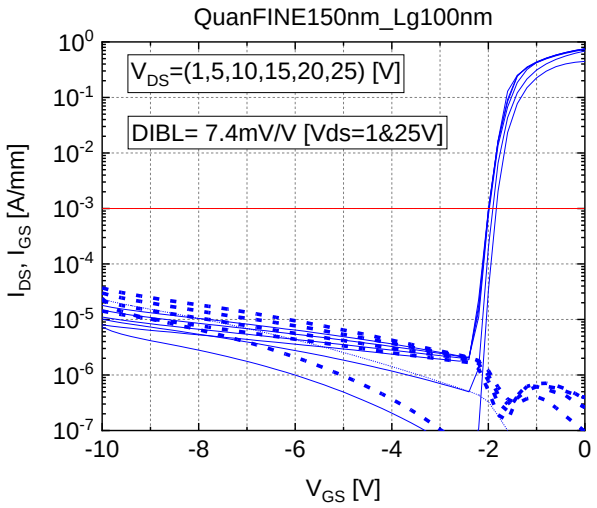
QuanFINE Beyond Ka-band

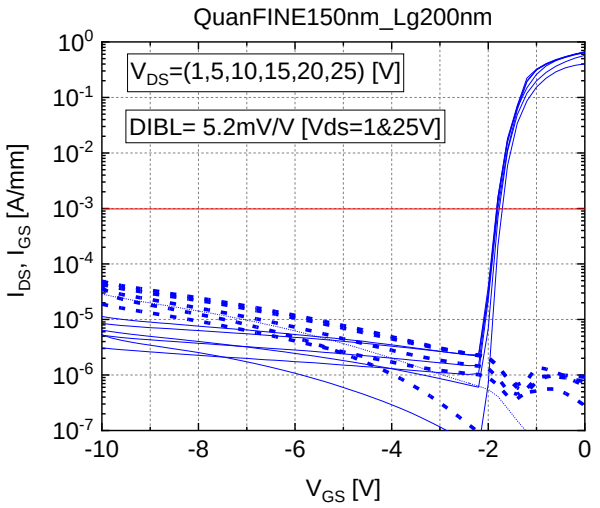
Motivation
Lack of good confinement epi for Lg100nm device

Summary
Lg100nm device with a good confinement is achieved on QF150

Future Work
- Material for Lg <100 nm

$GaN_{cap}/Al_{0.3}Ga_{0.7}N/AlN_{ex}$
150nm UID GaN layer
AlN NL
SiC substrate





$GaN_{cap}/Al_{0.3}Ga_{0.7}N/AlN_{ex}$
250nm UID GaN layer
AlN NL
SiC substrate