



# C3NiT

## Janzén

Swedish Center for III-Nitride Technology

# C3NiT day 2022

10<sup>th</sup> November 2022

## PROGRAM

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## ABSTRACTS

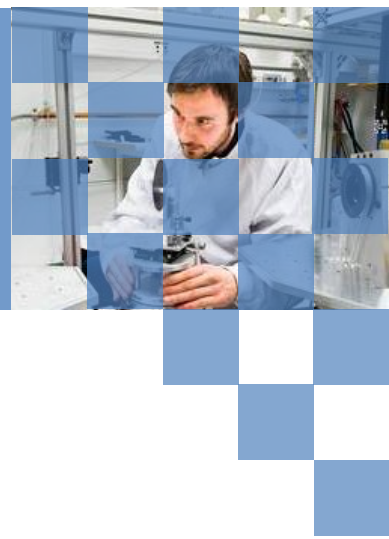


## PROGRAM

**Join in person:** Planck lecture hall, IFM, Linköping University

**Join by Zoom:** <https://liu-se.zoom.us/j/61485826379>  
(password via email: [philipp.kuhne@liu.se](mailto:philipp.kuhne@liu.se))

- 08.30 Welcome, Vanya Darakchieva, Centre Director, LiU
- 08.45 **Invited talk:** RF GaN HEMT Deep Levels and Reliability research at the University of Padova, Enrico Zanoni, University Padova
- 09.15 Project I: Advanced Epitaxial Growth, Vanya Darakchieva, LiU
- 09.30 PhD student and post doc project presentations
- 10.10 Break**
- 10.30 Project II: Vertical power devices, Mohammad Nawaz, HER/LiU
- 10.45 PhD student and Post doc project presentations
- 11.15 Project III: Lateral HEMTs for high frequency and power applications, Niklas Rorsman, Chalmers
- 11.30 **Invited talk:** *Towards GaN-on-GaN High-power Electronic Devices*, Michał Boćkowski, Polish Academy of Sciences
- 12.00 Lunch break**
- 13.00 **Relevance for industry I**, Trajan Bajdu, Gotmic
- 13.20 PhD student and post doc project presentations
- 14.30 Break**
- 14.45 Project IV: MMIC technology, Anna Malmros, Chalmers/Gotmic
- 15.00 Relevance for industry II**, Mattias Thorsell, SAAB
- 15.20 Project V: Developing next generation high-power  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> material, Daniela Gogova, LiU
- 15.35 **Invited talk**, Integration of GaN electronics with diamond, Joana Mendes, University of Aveiro
- 16.05 **Award Ceremony**
- 16.10 Closing Remarks, Niklas Rorsman, Chalmers
- 18:00 Dinner at Munkkällaren <https://www.munkkallaren.com/>



## ABSTRACTS

## INVITED SPEAKERS



## RF GaN HEMT Deep Levels and Reliability research at the University of Padova

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Gallium Nitride High Electron Mobility Transistors are essential components for high frequency, high power applications in the microwave and millimeter-wave range. The quest for higher bandwidth requires the scaling of these devices below the current values of gate length (100-250 nm). In order to avoid short-channel effects, the device structure has to be re-designed, introducing new materials for the barrier layer, like AlN, InAl(Ga)N or ScAlN, and improving carrier confinement and leakage current by adopting suitable GaN buffer compensation or back-barriers. In this presentation I will review the studies carried out at the University of Padova in the framework of European projects 5G\_GaN2 and EUGANIC, concerning deep levels and reliability of GaN-based HEMTs for RF applications with different design options.

### About the author:



**Enrico Zanoni** is professor of Microelectronics at the Department of Information Engineering of the University of Padova since 1993 and an IEEE Life Fellow. He and his group have been involved in research on the characterization, modeling and reliability of Gallium Nitride electronic and optoelectronic devices since 1999. At the University of Padova he contributed to establishing a microelectronics research group involved in CMOS analog and rf integrated circuit design, CMOS reliability and radiation hardness, compound semiconductor characterization, modeling, and reliability. The facilities of the associated laboratories include several systems for the DC, rf and pulsed characterization of GaN HEMTs, current Deep Level Transient Spectroscopy up to 600 V, accelerated testing in a wide range of environmental conditions, failure analysis using electroluminescence spectroscopy and microscopy techniques, AFM and electron microscopy. Various research projects at University of Padova deal with the study of reliability and failure physics of RF and power GaN HEMTs, GaN-based photodetectors, LEDs and lasers. Enrico Zanoni is coauthor of approximately one thousand publications on the modeling and reliability physics of silicon and compound semiconductor devices and of 4 patents.



## Towards GaN-on-GaN High-power Electronic Devices

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One of the best methods for introducing dopants into semiconductors is ion implantation. The introduced structural damage can be removed by a proper annealing process. The high-temperature treatment enables also electrical and/or optical activation of the implanted dopants. In the case of GaN, annealing at high temperature (~1300°C - 1400°C) seems difficult. This compound loses its thermodynamic stability slightly above 800°C at atmospheric pressure. At higher temperature the crystal will decompose. One of the solutions is to anneal GaN at high nitrogen (N<sub>2</sub>) pressure. Such technology is called ultra-high pressure annealing (UHPA). In this paper, the application of UHPA for GaN crystals and layers implanted by different ions (acceptors and donors) will be presented. The latest results of the implantation with magnesium (Mg), beryllium (Be), zinc (Zn), and calcium (Ca) ions into GaN in order to obtain p-type conductivity will be discussed. Silicon (Si) implantation into GaN for n-type doping will also be analyzed. Structural, electrical and optical properties of implanted GaN after UHPA will be discussed in terms of application for GaN-based devices.

### About the author:



**Michał Boćkowski** received the M.Sc. Eng. in Solid State Physics from the Warsaw University of Technology, Poland (1989), the Ph.D. in the Chemistry of Solids from the University Montpellier II, France (1995) and DSc in Physics from the Institute of Physics Polish Academy of Sciences (IP PAS), Poland (2013). He is currently a professor and the head of Crystal Growth Laboratory at the Institute of High Pressure Physics of the PAS (IHPP PAS). He is also a professor at the Center for Integrated Research of Future Electronics (CIRFE), Institute of Materials and Systems for Sustainability (IMaSS), Nagoya University (NU) as well as at the Institute of Global Innovation Research (IGIR), Tokyo University of Agriculture and Technology (TUAT), Japan. He has authored and co-authored more than 350 publications and presentations in scientific journals and conferences. His main interests are related to nitride semiconductors, material processing and crystal growth.



## Managing the heat of GaN HEMTs with diamond

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GaN high electron mobility transistors (HEMTs) are able to handle substantial power densities which result in highly-localized power densities and self-heating. The high temperatures decrease the MTTF, the performance, and the reliability of HEMTs – making the implementation of efficient thermal management techniques mandatory.

The transfer of heat from the hotspots to the package, where it can be ultimately dissipated to the heat sink or external environment, can be promoted by the use of materials with high thermal conductivity as substrates or chip-carriers. Due to its breakdown electric field and thermal conductivity, diamond is considered the ultimate thermal management material; it is available in the form of plates and can be deposited on non-diamond substrates, which allows for different possibilities of integrating it within the package.

The integration of GaN HEMTs and diamond films has been a research topic involving academic and industrial institutions for more than 20 years. The integration of both materials can be done in two ways: replacing the GaN substrate with diamond or capping the HEMT with a diamond film, close to the gate hotspot. The GaN-on-diamond wafers can be obtained by depositing the diamond film directly on the back of GaN layers, by bonding GaN HEMTs and diamond substrates, and by growing the GaN layers directly on diamond substrates (GaN epitaxy). This talk will describe each approach and will present their challenges and benefits. As a concluding remark, power amplifiers based on GaN-on-diamond technology are commercially available, attesting the potential and feasibility of integrating diamond and power components.

### About the author:



**Joana Catarina Mendes** received her Dipl-Ing and Dr-Phys degrees from the University of Aveiro, Portugal in 1998 and 2006, respectively. From 2006 to 2012, she was a researcher at the Nanotechnology Research Division in the Mechanical Engineering Department at the same University, where she worked with carbon-based nanostructured material composites and diamond films for tribological applications. Since 2012 Dr. Mendes works as a researcher in the Institute of Telecommunications. Her current interests are centred in the use of diamond films to improve the thermal management of high power high temperature electronic components and in biosensing applications. Dr. Mendes has participated in several national and international research projects, both as Principal Investigator and team member. She is the author or co-author of more than 50 journal and international conference papers and 6 book chapters. She is a permanent member of WOCSDICE Steering Committee.



# ABSTRACTS

## PhD Students & POST DOCS



## Anomalous transport properties of the two-dimensional electron gas in GaN-based high-electron-mobility transistor structures

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Understanding charge transport properties in nitride semiconductors often facilitates the production of more advanced electronic devices. Even though free charge carrier dynamics in semiconductors are well characterized, extended transport models are sometimes needed to describe the optical or electrical response of more complicated material systems. For example, a memory function model approach was used to derive a general Drude conductivity formula for quasi-two-dimensional boron nitride heterostructures, where the free electron scattering time is both temperature- and frequency-dependent [1]. Noble metals and other materials systems with high electron correlation also require extended Drude models to describe their free carrier response [2]. However, to the best of our knowledge, deviations from the classical Drude model have not been reported for two-dimensional electron gases (2DEG) inside semiconductor heterostructures with lower electron densities. Two previously published studies using terahertz spectroscopy show a strong temperature dependence of the 2DEG effective mass inside GaN-based high-electron-mobility transistor (HEMT) structures [3, 4]. This is not explained by any theoretical predictions and indicates more complicated electron transport mechanisms are at work. To further investigate this anomaly, we have performed terahertz optical Hall effect (THz-OHE) measurements on several GaN-based HEMTs with different barrier layer compositions ( $\text{Al}_{0.29}\text{Ga}_{0.71}\text{N}$ ,  $\text{In}_{0.14}\text{Al}_{0.86}\text{N}$ ,  $\text{AlN}$ ). For all these structures, the 2DEG effective mass shows a similar temperature dependence. We will discuss the possibility of a temperature- and frequency-dependent contribution to the effective mass and scattering time, which could be explained by extended Drude models or the memory function approach. These findings highlight the importance of measurement techniques like THz-OHE to evaluate these HEMT structures at the temperatures and frequencies which they will operate in future devices.

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## Fabrication of quasi-vertical GaN FinFETs on SiC substrates

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Wide bandgap semiconductors as gallium nitride (GaN) have gained research interest for high-voltage, high-power and high frequency application due to their large band gap, high critical field and high electron mobility [1]. Several device concepts have been presented, especially high electron mobility transistors (HEMTs), which consisting of a lateral device structure and are used commercially for some applications. However, the lateral structure suffers from heat dissipation and large areas are needed for power electronic current levels. The vertical structures are introduced where the BV is dependent on the drift layer thickness and not the lateral dimensions [2]. Further improvement could be achieved by confining the channel into a fin, to improve electrostatic control and obtain unipolar normally-off devices [3]. Further, the usage of GaN grown on foreign substrates gives a cost advantage in comparison to fully vertical structures.

Here, we present our work on the fabrication of quasi-vertical GaN FinFET on silicon carbide (SiC) substrates. The GaN layer stack was grown on SiC with hot-wall metalorganic chemical vapour deposition (MOCVD) technique, consisting of a n<sup>+</sup> (500nm)/n (2000 nm)/n<sup>+</sup> (100 nm) stack on an aluminum nitride (AlN) buffer layer. The fin was dry-etched with ICP-RIE with Cl<sub>2</sub>/BCl<sub>3</sub> gas masked by electron beam defined HSQ (FOX15) resist, followed by a TMAH wet etch to smoothen the sidewalls. The fin width and number per device was varied from 200 nm to 300 nm and 1 to 5 number of fins. A 100 nm bottom spacer of Al<sub>2</sub>O<sub>3</sub> was introduced to move the electrical field away from the fin edges and a 100 nm Al<sub>2</sub>O<sub>3</sub> top spacer to separate gate and source/drain contacts from each other, both grown with atomic layer deposition technique. The gate length was fabricated to around 350 - 500 nm in series with around 250 nm ungated fin regions above and below the gate and 1 μm bulk drift layer thickness. The gate stack consists of 80 nm tungsten (W) and 15 nm Al<sub>2</sub>O<sub>3</sub>, which was fabricated with ALD and sputter deposition, respectively. Before the gate oxide deposition, the GaN surface was treated with a digital etch consisting of alternating ozone treatment and HCl etch for 4 cycles, to improve the surface quality of the GaN ensuring a good interface quality to the gate oxide. For structuring of the different layers on the fin the resist planarization technique is used. Finally, a lift-off process for the sputtered Ti/Al/Ni/Au contact formation was performed.

The devices reveal low subthreshold slopes down to around 70 mV/dec indicating a good electrostatic control of the channel. For a 1 μm-thick drift layer, a low on-resistance below 0.05 mΩcm<sup>2</sup> (normalized on the fin area) and a breakdown voltage of 60 V was obtained. For devices with included post gate metallization annealing a decrease of the threshold voltage, reduced on-resistance and decreased by several orders of magnitude the gate leakage current compared to non-annealed devices. The devices showing ohmic contacts and slightly negative threshold voltages, which indicates normally-on behavior. The effective and field-effect mobility of the fin channel was obtained with a modeled carrier concentration and reveal to around 70 cm<sup>2</sup>/(Vs) and 13 cm<sup>2</sup>/(Vs) at high gate voltages, which is in a good comparison to so far reported similar devices.

By the introduction of an edge termination in the device fabrication process and a larger drift layer thickness we expect to reach higher breakdown voltages.

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## AlGaIn/GaN HEMTs for high frequency and high linearity applications

Alexis Papamichail<sup>1\*</sup>, Axel R. Persson<sup>1,2</sup>, Steffen Richter<sup>1,5,6</sup>, Philipp Kühne<sup>1,5</sup>, Vallery Stanishev<sup>1,5</sup>, Per O. Å. Persson<sup>1,2</sup>, Mattias Thorsell,<sup>3,4</sup> Hans Hjelmgren<sup>3</sup>, Niklas Rorsman<sup>3</sup>, Plamen P. Paskov<sup>1</sup>, and Vanya Darakchieva<sup>1,5,6</sup>

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III-nitride based high electron mobility transistors (HEMTs) provide unmatched potential for high power and high frequency circuits utilization in the rapidly evolving RF communication technology.<sup>[1]</sup> AlGaIn/GaN HEMTs with high power and current gain have been demonstrated in RF device applications. However, at high signal operation they show an inherent non-linear behavior which leads to gain compression and signal distortion.<sup>[2]</sup> Polarization-doped AlGaIn/GaN HEMTs, with a compositionally graded channel<sup>[3]</sup> enable a linear response improvement through formation of three-dimensional electron gas (3DEG),<sup>[4]</sup> which comes in tradeoff to mobility reduction due to alloy scattering in the AlGaIn channel. On the other hand, high power and ultra-high working frequencies are enabled by HEMT device scaling technologies. Such devices require high electron density in the two-dimensional electron gas (2DEG) and short gate-to-channel distance which can be realized by e.g. using high-Al-content ultra-thin barrier layers.<sup>[5,6]</sup> Furthermore, incorporation of a low-Al-content AlGaIn back barrier reduces the short channel effects and provides better electron confinement in the 2DEG channel. However, the growth of such structures by metalorganic chemical vapor deposition (MOCVD) is extremely challenging primarily due to the very small thickness and the high-Al content of the barrier layer.

In this work, we develop the growth process of compositionally graded channel HEMTs as well as high-Al AlGaIn/GaN HEMTs in a hot-wall MOCVD reactor. For the graded channel HEMTs, control of the graded profile is established through growth parameter tuning in combination with energy dispersive X-ray spectroscopy (EDS). Conventional and graded channel HEMTs were fabricated and compared in terms of device performance with the latter showing flat transconductance (and improved linearity) despite the ~50% decrease of mobility compared to the standard HEMT. Regarding the high-Al AlGaIn/GaN HEMTs, control of the thickness and the composition of a thin Al<sub>0.50</sub>Ga<sub>0.50</sub>N barrier layer is achieved. The HEMT structures were tested for aging with no signs of actual degradation. Next steps include development and fabrication of HEMTs with AlGaIn barrier layers with higher Al-content and simultaneous thickness reduction, and device evaluation.

### References

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## Quantifying Mg within GaN pyramidal domains: defects, detection, and doping

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High conductivity of semiconductors, useful for amongst others ohmic contacts, require high concentration of electrically active dopants.<sup>[1]</sup> For GaN however, the alternatives of p-dopants are limited.<sup>[2]</sup> Mg, the most useful p-dopant, suffers from high activation energy, and when used at high concentrations it is known to create structural defects. One such commonly observed defect is the pyramidal inversion domain (PID), a nm-sized structural domain within the GaN matrix with elevated Mg-levels.<sup>[3]</sup>

In this work we employ high-resolution scanning transmission electron microscopy (HR-STEM) to study samples of Mg-doped GaN grown by hot-wall metal-organic chemical vapor deposition (MOCVD).<sup>[4]</sup> Above a threshold of about  $2.4 \times 10^{19} \text{ cm}^{-3}$  the PIDs start to form, and these also vary in size with the total Mg concentration. Total net acceptor concentration drops with increased Mg after this threshold. The imaging in combination with sensitive spectroscopic mapping, through electron energy-loss spectroscopy (EELS), confirm the distribution of Mg at the interfaces of the PID. Therefore, a model of the whole structure can be compiled, including the positions of Mg.

We can show the Mg distribution and hence the total amount of Mg incorporated into these structures can be more accurately calculated. Capacitance-voltage (C-V) measurement of Mg in active sites, the total quantification of Mg through secondary ion mass spectrometry (SIMS) and the measured amount of Mg in PIDs can be compared for a series of samples to see if PIDs accounts for the drop in net-acceptor concentration or if there are other possible defects present.

### References

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## Thermal conductivity characterization of (Y, Sc)AlN alloys

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Alloying AlN with transition metals (i. e., Y, Sc) has been theoretically proved to strongly enhance spontaneous polarization of the material [1, 2]. Lattice engineering due to the alloying also enable lattice match with GaN while remaining large bandgap and strong spontaneous polarization. These properties of (Y, Sc)AlN alloys could offer a huge benefit for the development of GaN-based high-power (HP) and high-frequency (HF) electronic devices. For any electronic devices, especially working at HP, knowing of the thermal conductivity of the constituent materials and the heat transport through the structure of the devices is indispensable for the design and thermal management. Here, we report on the thermal conductivity of  $\text{Sc}_x\text{Al}_{1-x}\text{N}$  and  $\text{Y}_x\text{Al}_{1-x}\text{N}$  layers grown by magnetron sputter epitaxy on Si and sapphire substrates. Layers with a thickness of 300 nm and composition up to  $x = 0.22$  were examined. The thermal conductivity measurements were performed by transient thermoreflectance (TTR) in a temperature range of 100-400 K. All experimental data are interpreted by the Debye-Callaway model using the virtual crystal approximation. Phonon dispersion and mode Gruneisen parameters of binaries are obtained from *ab initio* calculations and interpolated for the alloys using Vegard's law to provide important inputs for the modeling. We observe a strong decrease of the thermal conductivity in the alloys with increasing Sc and Y compositions. This can be explained by the phonon-alloy scattering, which originates from the mass and size difference between the Al and Sc and Y atoms in the lattice. The strength of alloy scattering in  $\text{Y}_x\text{Al}_{1-x}\text{N}$  is found to be higher than that in  $\text{Sc}_x\text{Al}_{1-x}\text{N}$ , explaining the smaller thermal conductivity of  $\text{Y}_x\text{Al}_{1-x}\text{N}$  as compared to  $\text{Sc}_x\text{Al}_{1-x}\text{N}$  with an identical Y and Sc compositions. Temperature dependence measurements show that the thermal conductivity of both  $\text{Sc}_x\text{Al}_{1-x}\text{N}$  and  $\text{Y}_x\text{Al}_{1-x}\text{N}$  reaches a maximum at about 250 K and then saturates, which agrees well with the temperature independence of phonon-alloy and phonon-boundary scattering.

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## Homoepitaxial GaN growth under different nucleation schemes by hot-wall MOCVD

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The need to build a sustainable and efficient energy system motivates the development of vertical GaN transistors for applications with power ratings of 50-150 kW, e. g. in electric vehicles and industrial inverters. The key is to grow GaN layers with low concentration of defects (impurities and dislocations), which enables an expansion in both voltage and current ratings and reduction of cost. Since the growth of bulk GaN constitutes a challenge, the most used approach to develop GaN as an active material for optoelectronic and power applications has been its epitaxial growth on foreign substrates such as Si, sapphire and SiC [1]. The main limitations arising from this approach are the huge concentration of structural defects and residual strain. Recent improvements in GaN bulk growth by the ammonothermal [2] and HVPE methods [3] have allowed the homoepitaxial growth of GaN, which has the potential to result in a better quality of the GaN material due to the suppression of lattice and thermal mismatches. To fully exploit the potential of this approach, a deep understanding of the growth process is crucial to achieve the properties needed for practical applications.

In this work, we explore hot-wall MOCVD for the development and simultaneous GaN homoepitaxial growth on different GaN materials, which differ in threading dislocation densities and residual strain. Different growth modes are observed at growth temperature of 1020 °C – 3D island growth for GaN on GaN/AlN/SiC templates and layer-by-layer 2D growth for homoepitaxy on GaN HVPE substrate. These results are explained in terms of different origin of the atomic steps and different catalytic potential of GaN surface, which define the phenomena limiting the homoepitaxy - the kinetic advance of the steps and the adatom mobility, respectively. At reduced growth temperature, we also observe growth instabilities, which are explained in terms of the effects of the Ehrlich–Schwöbel energy barrier. The step-meandering growth transitions to step-flow growth when the growth rate is enhanced, which can be understood in view of growth kinetics. Extensive structural characterization shows that there was no generation of additional dislocations during homoepitaxial growth. GaN with smooth surfaces with a root mean square (RMS) value as low as 0.049nm and low background carbon concentration of  $5.3 \times 10^{15} \text{ cm}^{-3}$  has been achieved. In addition, we optimize and quantify the homoepitaxial growth in terms of the supersaturation with a comparison to the heteroepitaxial growth. Our results demonstrate the potential of the hot-wall MOCVD technique to deliver high-quality homoepitaxial GaN material for vertical power devices.

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## Limiting factors on 2DEG mobility in AlGa<sub>x</sub>N HEMTs with varying Al content

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AlGa<sub>x</sub>/Ga<sub>1-x</sub>N high-electron-mobility transistors (HEMTs) are important components in modern high-power/high-frequency electronics. Barrier layers with high Al-content  $x$  of Al<sub>x</sub>Ga<sub>1-x</sub>N are needed to downscale HEMTs that work beyond 250GHz at enhanced output power. It was found earlier that the mobility of the two-dimensional electron gas (2DEG) is optimal around 20% Al [1-4]. We employ optical Hall effect (OHE) measurements at below-THz frequencies [5,6], which allows to study the 2DEG properties, including effective electron mass, at room temperature. The study comprises a series of Al<sub>x</sub>Ga<sub>1-x</sub>N barrier layers with varying  $x$ , pseudomorphically grown on a GaN buffer by hot-wall metalorganic chemical vapor deposition. We obtain not only charge carrier density and mobility, but also effective mass or scattering time as a function of  $x$ . The latter are not accessible by other methods.

Good agreement is found for 2DEG density and mobility determined by the THz OHE with results from capacitance-voltage profiling, sheet resistance and DC Hall effect measurements. We find that mobility is generally reduced by about 25% as a result of an increased effective 2DEG mass. The level of the effective mass can approximately be explained by the accumulated effects of conduction-band nonparabolicity, polaron effect, and penetration of the wave function into the barrier. We confirm a mobility maximum around  $x=0.2$  and can trace its origin: At higher Al contents, the scattering time drops, indicating that mobility is lowered by increased scattering. For low Al contents, the scattering time remains generally long but the electron effective mass increases. HEMT structures with and without an additional AlN exclusion layer between the barrier and the channel will be compared to evaluate the effect of interface sharpness on the mobility.

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## Evaluation of SiC & GaN based power devices in a discrete cascade configuration for high power switching applications.

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Due to unique properties of wide bandgap (WBG) semiconductors [1], there is a huge potential in high power market such as electric vehicles (EV) and renewables where high frequency and high-power density is required. SiC based power devices have already made in-roads into commercial markets unlike GaN based power devices. GaN based power devices have huge potential for high power switching applications [1]. One of the challenges associated with high power GaN HEMTs is that majority of them are available as D-mode devices. This poses a unique challenge while working at system level design of power converters. The approach chosen here is to convert a D-mode normally-ON device into a normally-OFF configuration using discrete cascade. First, a commercially available High voltage D-mode SiC JFET along with Low voltage normally-ON Si MOSFET are used to mimic a discrete cascade topology. Necessary simulations are performed in LT-Spice to verify the switching requirements and then laboratory testing is done using a modified version of Solar Bora AB's half bridge converter setup. Once the functionality of Discrete cascade using D-mode SiC JFET was verified, the SiC JFETs are replaced with GaN HEMTs for the cascade configuration and necessary changes are made to the half bridge design. GaN HEMTs used here are based on SweGaN's QuanFINE® material. The switching behaviour of GaN HEMTs are tested under no load conditions and necessary results and conclusions regarding the challenges associated with cascade topology and GaN HEMTs are produced w.r.t. high power switching.

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## GaN MMIC real-time on-chip temperature monitoring and characterization

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Real-time on-chip temperature monitoring is of interest for GaN MMIC devices to allow better prediction of life-time under harsh operating conditions. The power density of the GaN technology is significantly higher than any other technology, especially for amplifier designs, which can lead to very large temperature gradients. A temperature monitoring method should be non-invasive, not affect device operation, and be fully compatible with industrialized device GaN foundry technologies. Furthermore, it should be indifferent to whether the device is bare-die or embedded. In order to achieve this, on-chip sensors and a novel calibration method have been developed, which enables real-time monitoring of a device. The method is tested by embedding sensors in a dedicated heater test structure for controlled power dissipation. The dedicated test dies were manufactured in the Chalmers in-house GaN process. By operating the sensor and the dedicated heating structure, we can not only monitor but also characterize the thermal properties of the complete epitaxial structure of the GaN technology. Furthermore, a detailed modeling of all the epitaxial layers and their interfaces results in accurate predictions of the measured temperature transients. This indicates the validity of the method and the potential use in the evaluation of embedding technologies.





## Investigation of Isolation Methods and the Stoichiometry of SiN<sub>x</sub> passivation layers in 'Buffer-free' GaN MISHEMTs for High Voltage Applications

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Gallium nitride (GaN) high electron mobility transistors (HEMTs) show remarkable electronic properties, including high critical electric field, mobility and saturation velocity, making them suitable for high-power microwave and power electronic applications. GaN-based heterostructures are typically grown on foreign substrates such as Si or SiC due to the high cost of GaN substrates. For high voltage power electronic HEMTs, Si is the most popular choice due to its low cost. However, the lattice mismatch between GaN and Si (or SiC) results in increased concentrations of extended defects, negatively impacting the electronic properties of the HEMT. The crystal quality can be improved by introducing strain relaxation layers and (Al)GaN buffer layers. In high voltage applications, the buffer layers must also be highly resistive to reduce off-state leakage currents. The resistivity of the buffer layers is typically increased by incorporating deep-level trap centres such as Fe or C that can compensate for unintentional n-type dopants such as Si and N vacancies in GaN. Furthermore, GaN grown on conductive substrates must have sufficiently thick buffer layers to prevent vertical breakdown. Introducing C or Fe close to the active region also entails more dynamic R<sub>on</sub> dispersion when switching from a high voltage off-state to a high current on-state. In this work, we instead use a GaN-on-SiC heterostructure that doesn't require a thick buffer layer. This 'buffer-free' heterostructure, termed QuanFINE®, effectively eliminates C and Fe-related traps while providing good vertical isolation in the semi-insulating SiC substrate. We have used this heterostructure to fabricate high voltage metal-insulator-semiconductor HEMTs (MISHEMTs). Silicon nitride (SiN<sub>x</sub>) deposited using low-pressure chemical vapor deposition (LPCVD) was utilized as a passivation layer due to its effectiveness in reducing surface traps and its good insulating properties. The HEMT device performance is tested for two SiN<sub>x</sub> layers with different stoichiometry. We demonstrate devices with gate leakage currents below 10 nA/mm at 1000 V by utilizing a more stoichiometric SiN<sub>x</sub> passivation. Mesa isolation and nitrogen implantation isolation was also compared. It was possible to achieve breakdown voltages over 2000 V by employing nitrogen implantation, whereas mesa isolation was limited below 1500 V. These results show the potential of the 'buffer-free' heterostructure for high voltage applications.



## Hot-wall MOCVD of N-polar group-III nitride materials and high electron mobility transistor structures

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Recently, nitrogen (N)-polar III-nitride wide-bandgap semiconductor materials have attracted considerable attention in optoelectronic and electronic device applications. In particular, compared to conventional gallium (Ga)-polar high electron mobility transistor (HEMT) structures, N-polar HEMTs exhibit superior performance, such as the feasibility to fabricate low resistive ohmic contacts, an enhanced carrier confinement with a natural back barrier, as well as better device scalability [1]. Previous study shows that the presence of hexagonal hillocks that causing high surface roughness has been successfully suppressed by employing certain offcut angles on substrates [2]. To further enhance the surface morphology, a two-step temperature growth process or a high V/III ratio are typically used [2][3]. However, step-bunching is still present and affects device performance, especially in case of GaN/AlGaN/GaN heterostructures that require sharp interfaces for optimized two-dimensional electron gas (2DEG). Besides, the polarity affects material properties such as impurity incorporation, surface roughness, defects. Unintended formation of polarity inversion domains (IDs) is the typical type of defects in N-polar epitaxial layers and device heterostructures. The cause of IDs in most case is attributed to impurity incorporation, such as oxygen [4]. Effectively, local polarity IDs also deteriorate the crystal quality and, thus, device performance. Therefore, it is critical to reliably determine and control the polarity of III-nitride epilayers and device heterostructures.

In this work, we present new evidence that showing limitations of KOH and XRD techniques in determining the polarity of mixed-polar III-nitrides [5]. We show a comprehensive structural investigation with both atomic detail and thermodynamic analysis of the polarity evolution in low- and high-temperature AlN layers on on-axis and 4° off-axis Carbon-face 4H-SiC (000-1) grown by hot-wall metal organic chemical vapor deposition (MOCVD). A polarity control strategy has been developed by variation of thermodynamic Al supersaturation and substrate misorientation angle in order to achieve desired growth mode and polarity. We demonstrate that IDs are totally suppressed for high-temperature AlN nucleation layers when step-flow growth mode is achieved at the off-axis. We employ this approach to demonstrate high quality N-polar epitaxial AlGaN/GaN/AlN heterostructures. We have further optimized growth process of N-polar GaN epitaxial layers with the effect of the different substrate misorientation angles. Compared with 2-step growth process, multi-step temperature growth results in better crystalline quality regarding both surface roughness and dislocation density. Smooth surfaces with root mean square (RMS) of 1.4 nm and 0.5 nm over 5 μm × 5 μm scanning area were obtained for GaN grown on SiC off-cut towards the a-plane and m-plane, respectively. A growth strategy employing 4-step temperature process is proposed and demonstrated to eliminate step bunching. Finally using the 4-step growth process N-polar GaN/AlGaN/GaN HEMT structures were demonstrated with 2DEG carrier density as high as 10<sup>13</sup> cm<sup>-2</sup>. The 2DEG mobility ( $\mu_x = 1170$  cm<sup>2</sup>/V·s;  $\mu_y = 820$  cm<sup>2</sup>/V·s at room temperature), determined by terahertz optical Hall effect was found to be anisotropic. We further proved the potential of using hot-wall MOCVD to deliver high quality N-polar III-nitride layers and device quality structures.

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## Electron effective mass in bulk GaN

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Despite GaN quickly becoming one of the mainstream technologies in electronic and optoelectronic devices, there are still some fundamental questions remaining about the material properties that have not been answered. Strong temperature dependence of the electron effective mass parameter of the two-dimensional electron gas (2DEG) in GaN-based high electron mobility transistor structures (HEMTs) has been reported recently by using the terahertz (THz) optical Hall effect (OHE) [1, 2] and 2D plasmon resonance measurements [3]. This is an important parameter that provides insight into the factors limiting electron mobility in GaN. The existing reports focus on HEMTs, where the electrons are confined at the interface between GaN and the barrier layer. However, it remains unclear whether the effective mass temperature dependence is some unique property limited to electrons confined in a two-dimensional channel or it also extends to the case of free electrons in bulk GaN.

In this work, we report a study of the electron effective mass parameter in bulk GaN at various temperatures using the THz and mid-infrared (MIR) OHE [4, 5]. We measured Si-doped epitaxial GaN layers ( $5 \times 10^{17} \text{ cm}^{-3}$  and  $5 \times 10^{18} \text{ cm}^{-3}$ ) on 4H-SiC substrates grown by hot-wall MOCVD and bulk n-type GaN substrate ( $[\text{Si}] = 1 \times 10^{17} \text{ cm}^{-3}$ ). The free electron concentration and resistivity determined by the THz OHE are found to be in very good agreement with results obtained by the electrical Hall effect measurements. The electron effective mass parameter determined by the THz OHE at room temperature was found to be  $(0.34 \pm 0.01)m_0$  and  $(0.42 \pm 0.06)m_0$  for epitaxial layers and GaN substrate, respectively. These values are significantly higher than the value of  $(0.22-0.23)m_0$  typically reported in the literature. Our THz OHE results further reveal that at low temperatures ( $<100 \text{ K}$ ) the electron effective mass is  $(0.20-0.22)m_0$  and it exhibits a strong temperature dependence similar to that reported for HEMTs [1-3]. In contrast, the electron effective mass parameter in epitaxial GaN determined by the MIR OHE is  $0.20 m_0$  at both low and high temperatures. We discuss our results in comparison to effective mass dependence reported for GaN-based HEMTs and go through the possible mechanisms that could lead to effective mass enhancement in GaN such as band structure nonparabolicity, electron-phonon coupling, and deviation from the Drude behavior.

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## Investigation of leakage path in buffer-free heterostructure

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GaN based high electron mobility transistors (HEMTs) have been considered as a promising candidate for next generation high frequency and high power electronic devices. However, the leakage current is a critical problem that limits the performance of the device. In conventional epi-structure, carbon (C) or iron (Fe) doping is needed to ensure the insulation of GaN buffer and mitigate leakage currents, but with the trade-off of trapping effects. A novel approach, QuanFINE, which is a “buffer-free” heterostructure that completely removes the thick C-/Fe-doped buffer to reduce the trapping effects and provides desired 2DEG confinement by AlN nucleation layer. However, due to the removal of C-/Fe-doped buffer layer, potential leakage path may occur. Therefore, the goal of this work is to seek and identify whether there are any potential leakage paths in QuanFINE. Low frequency s-parameters were measured on a new leakage test structure on samples with different GaN channel thicknesses. An equivalent circuit model was developed based on the measured s-parameters in advanced design system (ADS). The relationship between extracted parameters (capacitance, inductance, and resistance) and GaN channel thickness were analyzed.



## High Temperature Annealing Impact on First Passivation Fluorine Etched Gate Recessed AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT

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With the overarching goal of attaining mm-wave Ga<sub>N</sub> High Electron Mobility Transistors (HEMTs) (W-band and above), vertical and lateral downscaling is of essence. Whereas gate-length ( $L_g$ ) downscaling, yields lower electron transit time, it also causes undesirable short-channel effects (SCE), which can be counteracted by vertical downscaling enabling a preserved gate control [1]. Utilizing Passivation first technology (coupled with mini-FP T-gates), Schottky Gate (SG) is formed by Fluorine plasma over-etching, where the plasma etching allows highly defined nanoscale  $L_g$  features. Nevertheless, the over-etching of the SiN<sub>x</sub> entails F-plasma exposure to the Ga<sub>N</sub> cap layer which generates considerable modification of surface chemistry, etching and F-implantation which may cause positive threshold voltage ( $V_{TH}$ ) -shift [2], but also lead to device reliability issues [3].

Gate recess dry etching, using NF<sub>3</sub> or CF<sub>4</sub> Inductive Coupled Plasma (ICP) on SiN<sub>x</sub> is here studied with respect to the impact etching has on the AlGa<sub>N</sub>/Ga<sub>N</sub> High Electron Mobility Transistor (HEMT) IV performance, such as  $V_{TH}$ . Additionally, high temperature pre gate annealing (PGA) at 600 – 800°C is employed to evaluate at what degree the adverse effects of over-etching, (crystal structure degradation and Fluorine implantation) may be reversed. Atomic Force Microscopy (AFM) and X-ray Photoelectron Spectroscopy (XPS) are employed to help characterize the mechanisms behind the change in IV-performance caused by the F-plasma and/or the PGA treatment.

It is found that the plasma chemistry highly impacts the effect over-etching of the gate recess may have, considering CF<sub>4</sub>-plasma, there hitherto exists misconceptions of what mechanisms lie behind the positive  $V_{TH}$ -shift, many articles overestimate the role implanted F<sup>-</sup> ions has while the etching of the top barrier is not considered [4]–[8], or underestimated [2], [9]. This study helps to shed light on both mechanisms role in the  $V_{TH}$ -shift. Over-etching with NF<sub>3</sub>-plasma does not etch Ga<sub>N</sub> and has a much smaller impact on the  $V_{TH}$  but is nonetheless shown to change the surface chemistry and lead to F-implantation. Whereas PGA can to a certain extent reverse the adverse effects CF<sub>4</sub>-plasma had on the IV-characteristics, PGA on the NF<sub>3</sub>-plasma etched gate recesses show minor impacts.

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